Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A multiplying digital-to-analog converter comprising:

a plurality of multiplying cells, wherein each multiplying cell is connected to a differential local oscillator bias signal voltage;

a local oscillator transmission line wherein said differential local oscillator bias signal voltage is provided on said local oscillator transmission line, and each of said plurality of multiplying cells is connected to said local oscillator transmission line;

a digital input including a plurality of bits, wherein each bit is connected to a binary-weighted number of said multiplying cells; [[and]]

an output connected to each of said plurality of multiplying cells, wherein a differential output current is provided at said output; and

an output transmission line wherein:

said output is provided on said output transmission line; and

each of said local oscillator transmission line and said output transmission lines has a propagation delay and said propagation delays are matched.

2. (canceled)

3. (canceled)

4. (original) The multiplying digital-to-analog converter of claim 1 wherein:

said plurality of bits of said digital input forms a digital word having a value b_n;

each of said plurality of multiplying cells establishes a differential local oscillator current (i_{LO}); and

said differential output current is the product of said value b_n and said differential local oscillator current (i_{LO}).

5. (original) The multiplying digital-to-analog converter of claim 1 wherein:

said differential output current is the sum of a plurality of differential output currents of the plurality of multiplying cells.

6. (original) The multiplying digital-to-analog converter of claim 1, further comprising:

a plurality of bit lines wherein:

each bit of said digital input is provided on a distinct one of said plurality of bit lines;

each bit has a significance from most significant to least significant; and

a binary-weighted number of multiplying unit cells is connected to at least one bit line of said plurality of bit lines, wherein said binary-weighted number matches the significance of the bit of said bit line.

7. (original) The multiplying digital-to-analog converter of claim 1, further comprising:

a plurality of bit lines wherein:

each bit of said digital input is provided on a distinct one of said plurality of bit lines;

each bit has a significance from most significant to least significant; and

a multiplying interpolation cell is connected to at least one bit line of said plurality of bit lines, wherein said interpolation cell provides an output level that matches the significance of the bit of said bit line.

8. (original) The multiplying digital-to-analog converter of claim 1, further comprising:

a plurality of bit lines wherein:

each of said plurality of bit lines has a propagation delay and said propagation delays are matched.

9. (original) The multiplying digital-to-analog converter of claim 1, further comprising:

a local oscillator transmission line;

an output transmission line; and

a plurality of bit lines wherein:

each of said local oscillator transmission line, said output transmission line, and each of said plurality of bit lines has a propagation delay and all of said propagation delays are matched.

10. (original) The multiplying digital-to-analog converter of claim 1 wherein:

said plurality of multiplying cells are component-matched identical cells.

11. (original) A multiplying cell comprising:

a local oscillator input that receives a continuous time local oscillator input signal;

a digital input that receives a single bit digital input;

a balanced output, having a constant output impedance, that yields a differential output current signal, said differential output current signal being the multiplication of said continuous time local oscillator input signal by said single bit digital input.

12. (original) The multiplying cell of claim 11, further comprising:

a pair of current sources connected to said continuous time local oscillator input signal, where said pair of current sources establish a differential local oscillator current.

13. (original) The multiplying cell of claim 11, further comprising:

a pair of current sources connected to said continuous time local oscillator input signal, where said pair of current sources establish a differential local oscillator current; and

two sets of current switches connected to said current sources and to said digital input, wherein said sets of current switches toggle the direction of said differential local oscillator current at said balanced output to yield said differential output current signal, and said sets of current switches toggle the direction of said differential local oscillator current based on the state of said single bit digital input.

14. (original) The multiplying cell of claim 11 wherein the impedance of said digital input is high.

15. (original) The multiplying cell of claim 11 wherein the impedance of said local oscillator input is high.

16. (original) The multiplying cell of claim 11 wherein the impedance of said balanced output is high and constant.

17. (original) The multiplying cell of claim 11 further comprising an attenuator across said local oscillator input and wherein said differential output current signal is provided at a different additional level to provide an interpolation bit.

18. (original) A multiplying cell comprising:

a pair of current sources fed at a local oscillator input by a differential local oscillator bias signal voltage $V_{DC} \pm v_{LO}$ and that establish a differential local oscillator current i_{LO} superimposed on a DC bias level I_{DC};

two sets of current switches connected to said current sources and having a digital input receiving an input signal comprising a bit having states H and L, wherein:

said sets of current switches provide a differential output current signal I_{out} at a balanced cell output having an outl output and an outh output;

$I_{out} = I_h - I_l$ where I_h is the output current at the outh output and I_l is the output current at the outl output; and

I_{out} is a positive multiple of i_{LO} when said bit has state H and I_{out} is a negative multiple of i_{LO} when said bit has state L.

19. (original) The multiplying cell of claim 18 wherein:

said input signal has a bit rate exceeding 1.0 Gbit/s.

20. (original) The multiplying cell of claim 18 wherein:

said differential local oscillator bias signal voltage has a frequency of about 1.0 GHz or higher.

21. (original) The multiplying cell of claim 18 wherein:

said multiplying cell has high and constant impedances at said local oscillator input, said digital input, and said balanced cell output.

22. (original) The multiplying cell of claim 18 wherein:

the multiplying cell is a unit cell and $I_{out} = +2i_{LO}$ when said bit has state H and $I_{out} = -2i_{LO}$ when said bit has state L.

23. (original) The multiplying cell of claim 18 further comprising:

a resistive attenuator, said resistive attenuator being tapped to feed a differential local oscillator bias signal voltage $V_{DC} \pm Kv_{LO}$ to said pair of current sources; and

the multiplying cell is an interpolation cell and $I_{out} = +2Ki_{LO}$ when said bit has state H and $I_{out} = -2Ki_{LO}$ when said bit has state L.

24. (original) A traveling wave, multiplying digital-to-analog converter comprising:

a local oscillator transmission line wherein said differential local oscillator bias signal voltage is provided on said local oscillator transmission line;

an output transmission line;

a plurality of multiplying cells, wherein:

each of said plurality of multiplying cells is connected to said local oscillator transmission line and to said output transmission line;

each of said plurality of multiplying cells establishes a differential local oscillator current (i_{LO}); and

propagation delays at each multiplying cell are matched between said local oscillator transmission line and said output transmission line so that a plurality of output signals from each multiplying cell combine in phase on said output transmission line; and

a plurality of control lines providing a digital input including a plurality of bits wherein each bit is connected to said multiplying cells so that said multiplying cells provide a differential output current on said output

transmission line that is a product of a binary weighting of said plurality of bits and said differential local oscillator current (i_{LO}).

25. (original) The traveling wave, multiplying digital-to-analog converter of claim 24 wherein:

said plurality of multiplying cells are connected to said plurality of control lines so that multiplying cells connected to one bit of said plurality of bits are interleaved among all other multiplying cells of said plurality of cells.

26. (original) The traveling wave, multiplying digital-to-analog converter of claim 24 wherein:

said plurality of multiplying cells are connected to said plurality of control lines so that spatial averaging of said plurality of bits from most significant bit to least significant bit maintains linearity of digital-to-analog conversion in the presence of any linear gradient across the plurality of multiplying cells.

27. (original) A satellite transponder comprising:

a traveling wave multiplying digital-to-analog converter having propagation-delay matched transmission lines and having an array of high and constant impedance multiplying cells for conversion of a high bandwidth digital input to a high frequency RF analog output wherein said array of high and constant impedance multiplying cells are connected along said transmission lines that propagate said high frequency RF analog output and along bit lines that propagate said high bandwidth digital input.

28. (original) The satellite transponder of claim 27 wherein said array of multiplying cells are identical component-matched multiplying cells having nominally identical impedances and propagation delays so that a plurality of output signals from each multiplying cell combine in phase on at least one of

said transmission lines.

29. (original) The satellite transponder of claim 27 wherein said array of multiplying cells are interleavedly connected along said bit lines so that linearity of digital to analog conversion is preserved in the presence of any linear gradient δ from one cell to another across said array of multiplying cells

30. (original) The satellite transponder of claim 27 wherein said high frequency is at least as high as a microwave frequency.

31. (original) The satellite transponder of claim 27 wherein said high bandwidth digital input has a bit rate of at least 1.0 Gbit/s.

32. (original) The satellite transponder of claim 27 wherein said digital input has a resolution of at least three bits.

33. (original) The satellite transponder of claim 27 wherein a multiplying cell of said array of multiplying cells includes:

a local oscillator input that receives a continuous time local oscillator input signal;

a digital input that receives a single bit digital input; and

a balanced output, having a constant output impedance, that yields a differential output current signal, said differential output current signal being the multiplication of said continuous time local oscillator input signal by said single bit digital input.

34. (currently amended) A method for digital-to-analog conversion comprising steps of:

<u>propagating a differential local oscillator bias signal voltage along a local oscillator transmission line;</u>

feeding each of a plurality of multiplying cells [[a]] <u>said</u> differential local oscillator bias signal voltage;

providing a digital input including a plurality of bits;

connecting each bit to a binary-weighted number of multiplying cells of said plurality of multiplying cells;

connecting an output to each of said plurality of multiplying cells; and

providing a differential output current at said output.

35. (canceled)

36. (currently amended) The method of claim <u>34</u> [[35]] further comprising steps of:

propagating said differential output current along an output transmission line; and

matching propagation delays of said local oscillator transmission line and said output transmission line.

37. (original) The method of claim 34 further comprising steps of:

establishing a differential local oscillator current (i_{LO}); and

forming said differential output current as the product of a value b_n and said differential local oscillator current (i_{LO}) wherein said plurality of bits of said digital input forms a digital word having said value b_n.

38. (original) The method of claim 34 further comprising a step of:

forming said differential output current as the sum of a plurality of differential output currents of the plurality of multiplying cells.

39. (original) The method of claim 34 further comprising steps of:

providing each bit of said digital input on a distinct one of a

plurality of bit lines, wherein each bit has a significance from most significant to least significant; and

connecting each bit line to a binary-weighted number of multiplying unit cells, wherein said binary-weighted number matches the significance of the bit of said bit line.

40. (original) The method of claim 34 further comprising steps of:

providing each bit of said digital input on a distinct one of a plurality of bit lines, wherein each bit has a significance from most significant to least significant; and

connecting at least one bit line of said plurality of bit lines to a multiplying interpolation cell, wherein said interpolation cell provides an output level that matches the significance of the bit of said at least one bit line.

41. (original) The method of claim 34 further comprising steps of:

providing said plurality of multiplying cells as component-matched identical cells; and

matching propagation delays along a local oscillator transmission line, an output transmission line, and a plurality of bit lines.

42. (original) A method for direct bits-to-RF digital-to-analog conversion comprising steps of:

propagating a local oscillator signal along an input transmission line;

propagating a digital input signal along a plurality of bit control lines, said digital input signal comprising a plurality of bits, and said plurality of bits forming a digital word having a value b_n;

connecting a plurality of multiplying cells to said input transmission line and to an output transmission line, each of said plurality of multiplying cells establishing a differential local oscillator current; and

toggling said differential local oscillator currents on said output transmission line using said multiplying cells so that a differential output current is the product of said value b_n and said differential local oscillator current.

43. (original) The method of claim 42 wherein said connecting step comprises matching propagation delays of said multiplying cells between said input transmission line and said output transmission line.

44. (original) The method of claim 42 wherein said digital input signal has a resolution of at least three bits.

45. (original) The method of claim 42 wherein:

said digital input signal has N bits;

said plurality of multiplying cells includes a number m of interpolation cells; and

the number of said plurality of multiplying cells is $(2^{N-m} - 1) + m$.

46. (original) The method of claim 42 wherein said local oscillator signal has a frequency at least as high as a microwave frequency.

47. (original) A communication system comprising:

a traveling wave, multiplying digital-to-analog converter for conversion of a digital input to a high frequency analog output, said digital-to-analog converter having propagation-delay matched transmission lines wherein:

an array of constant high impedance, multiplying cells are connected along said transmission lines, at least one of which propagates said high frequency analog output; and

said array of constant high impedance, multiplying cells are connected along bit lines that propagate said digital input.

48. (original) The communication system of claim 47 wherein said array of multiplying cells are interleavedly connected to said bit lines so that linearity of digital to analog conversion is preserved in the presence of a linear gradient δ from one cell to another across said array of multiplying cells.

49. (original) The communication system of claim 47 wherein said array of multiplying cells are identical component-matched multiplying cells having nominally identical impedances and propagation delays so that a plurality of output signals from each multiplying cell combine in phase on at least one of said transmission lines.

50. (original) The communication system of claim 47 wherein said high frequency is at least 1.0 GHz.

51. (original) The communication system of claim 47 wherein said digital input has a data rate of at least 1.0 Gbit/s.

52. (original) The communication system of claim 47 wherein said digital input has a resolution of at least three bits.

53. (original) The communication system of claim 47 wherein a multiplying cell of said array of multiplying cells includes:

a local oscillator input that receives a continuous time local oscillator input signal;

a digital input that receives a single bit digital input; and

a balanced output, having a constant output impedance, that yields a differential output current signal, said differential output current signal being the multiplication of said continuous time local oscillator input signal by said single bit digital input.